REMARKS/ARGUMENTS

Claims 3-4 and 18-27 are pending in the application.

Claims 23-27 were rejected under 35 U.S.C. §102(b) as being anticipated by Papathomas et al., U.S. Patent No. 5,656,862 (hereinafter "Papathomas"). Claims 3-4 and 18-22 were allowed.

Figure 1 has been designated and identified as Prior Art to comply with the Examiner's request. Replacement sheets 1-13 are attached following page 7 of this paper.

Claim Rejections Under 35 U.S.C. §102(b)

Claims 1, 5, 7, 14, and 18 were rejected under 35 U.S.C. §102(b) as being anticipated by Papathomas. Papathomas generally discloses a solder interconnection encapsulant, encapsulated structure and method for its fabrication and use (*See* Abstract).

Papathomas does not disclose filler particles dispersed in the benzocyclobutene, as recited by claims 23 and 25. The relevant sections of Papathomas state:

> In the figure, numeral 1 represents a semiconductor chip joined to the chip carrier 2 by solder bumps 3 mated to pads 4. I/O can be in the form of pins extending and protruding from the carrier 2, with a small portion of the pins protruding from the other side of the carrier for carrying current thereto.

(*See* Papathomas, Col. 3, Lines 51-53).

> The encapsulant 5 pursuant to the present invention provides for essentially void free encapsulation of the solder connections thereby assuring highly reliable devices and fills the gap forming a uniform fillet around the chip as well as covering the pin heads, circuits, vias, or solder masks under the device (not shown).

(*See* Papathomas, Col. 3, Lines 62-67).

In other words, solder bumps 3 are surrounded by an encapsulant 5, as opposed to filler particles dispersed in the benzocyclobutene. Therefore, Papathomas does not disclose filler particles dispersed in the benzocyclobutene. Applicants respectfully submit, therefore, that elements of claim 23 and 25 are neither shown nor suggested by the cited reference. Claims 24 and 26-27 depend from claims 23 and 25, respectively. Accordingly reconsideration and withdrawal of the rejection of claims 23-27 under 35 U.S.C. §102(b) is respectfully requested.

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

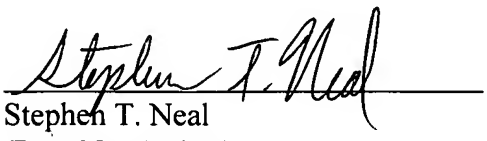
The Commissioner is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

Respectfully submitted,

KENYON & KENYON

Dated: April 11, 2005

By: 
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(Reg. No. 47,815)
Attorneys for Intel Corporation

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San Jose, CA 95110

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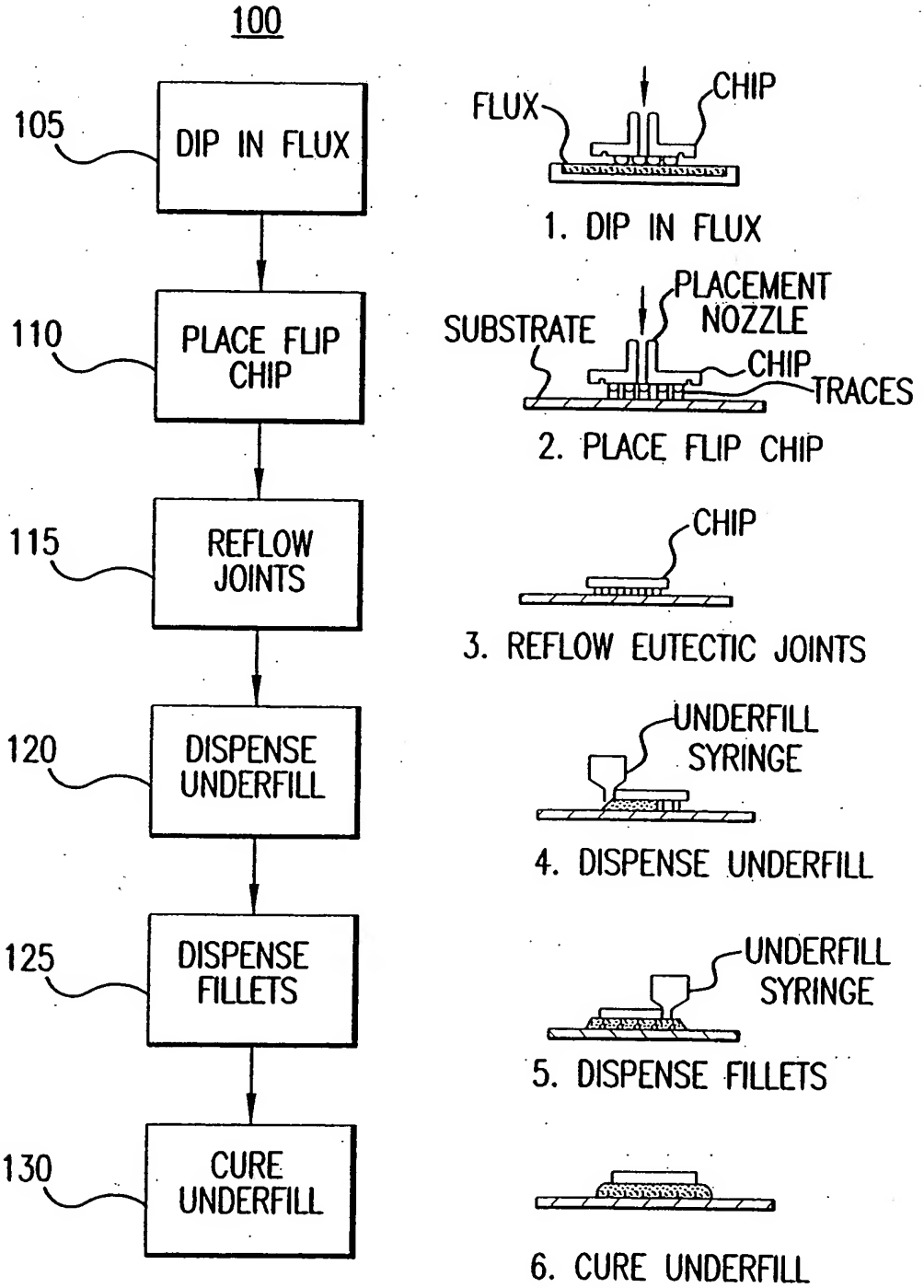

FIG. 1
(Prior Art)

200

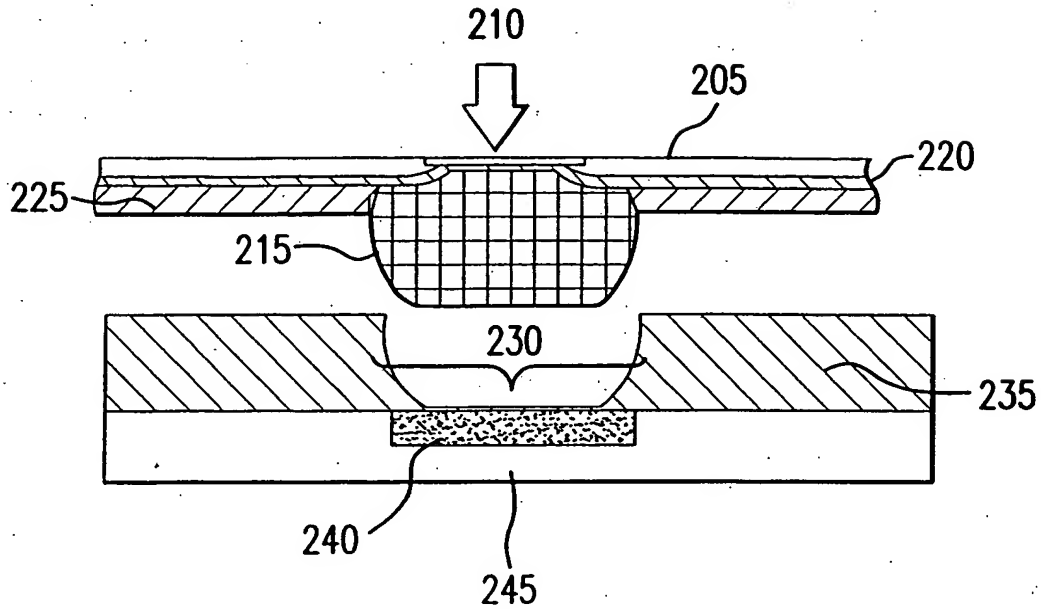

FIG.2

300

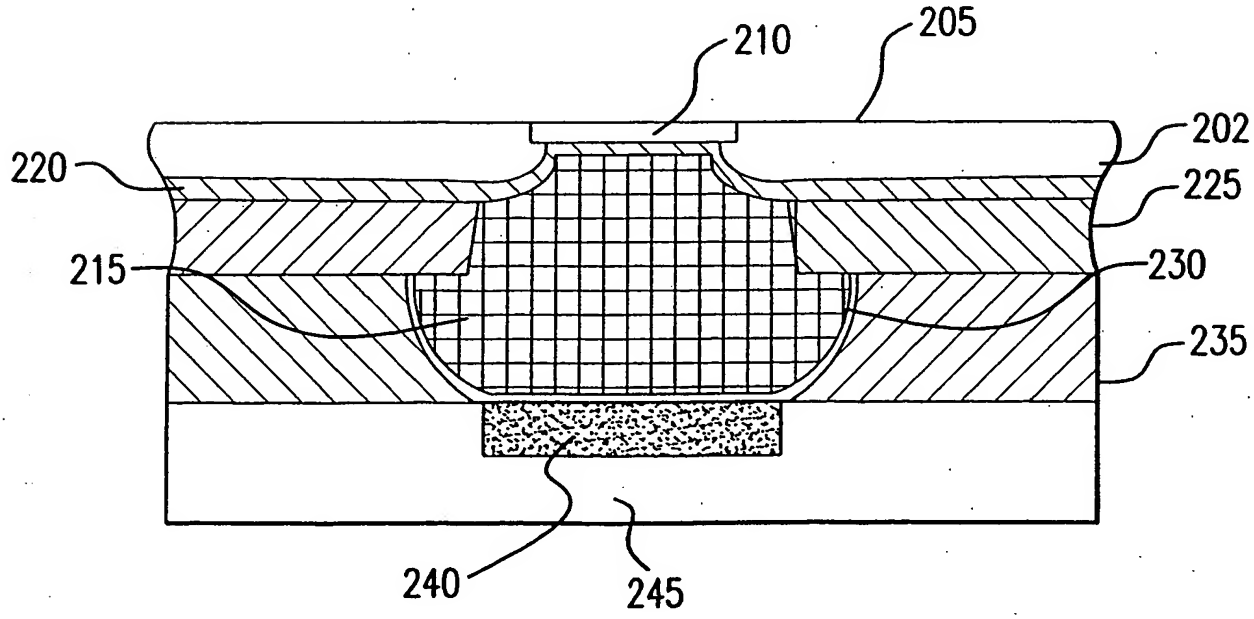

FIG.3

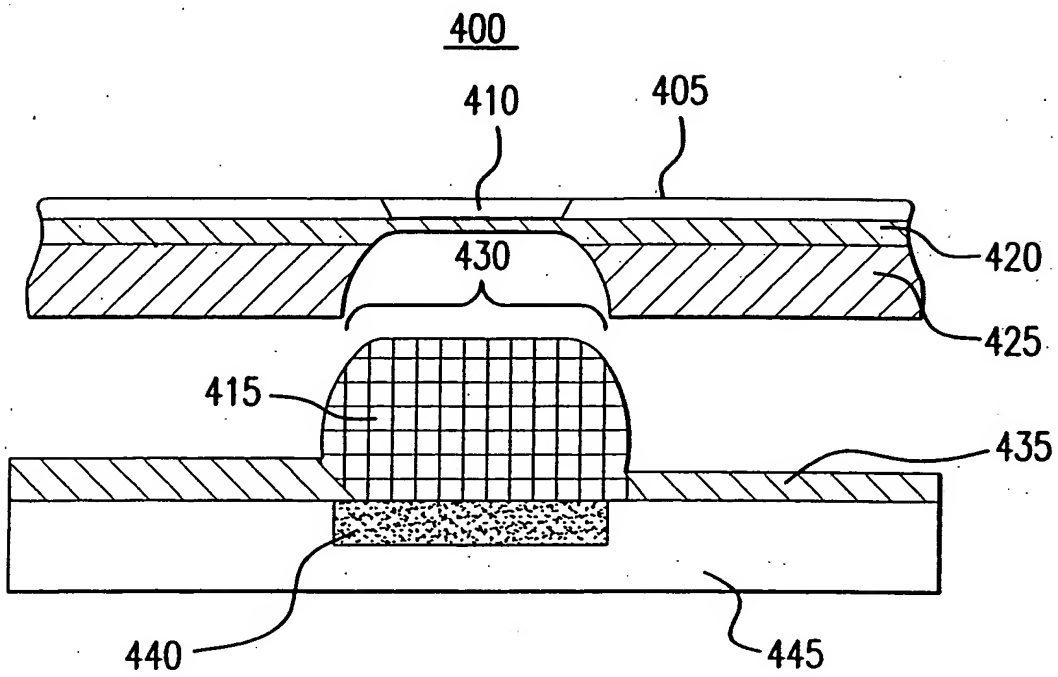
400
410
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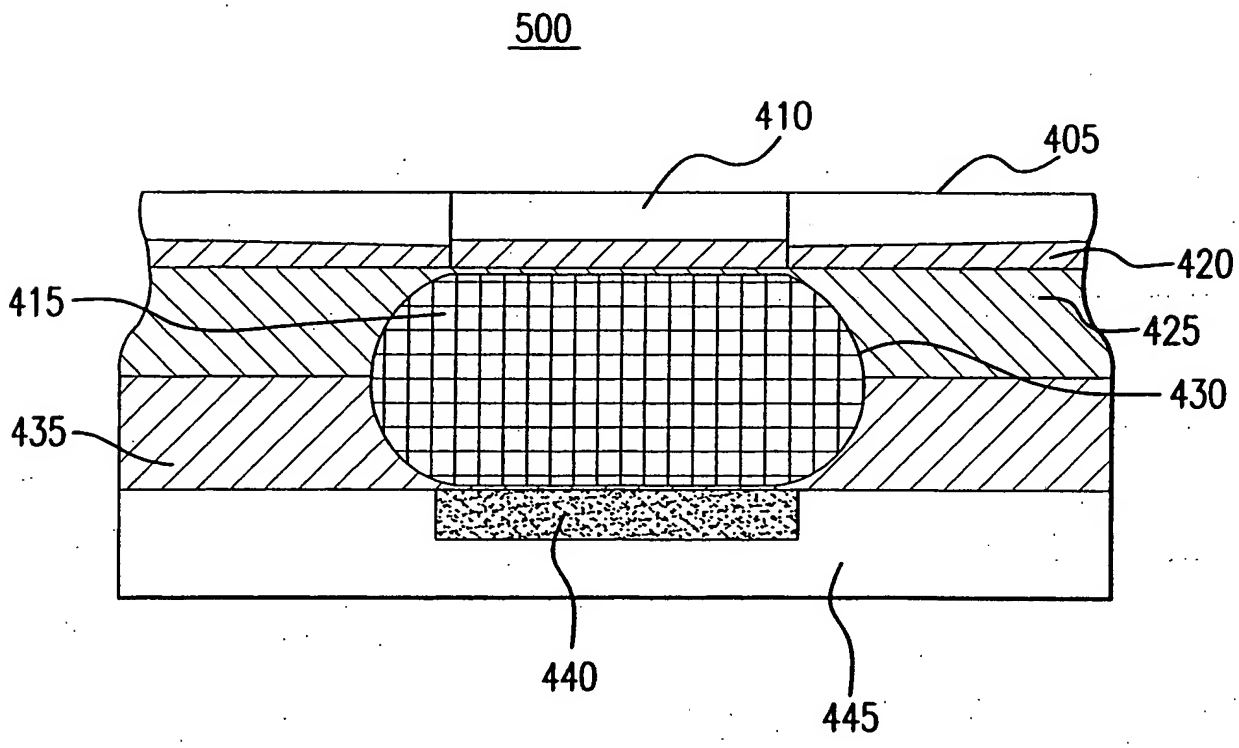
FIG.4


500
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440
445

FIG.5

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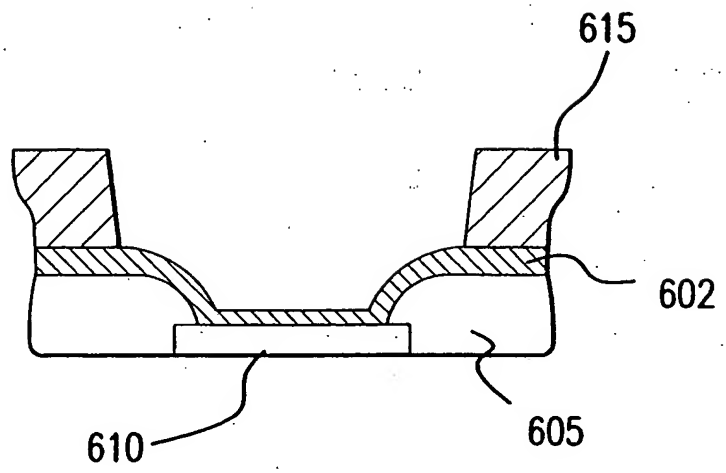

FIG.6

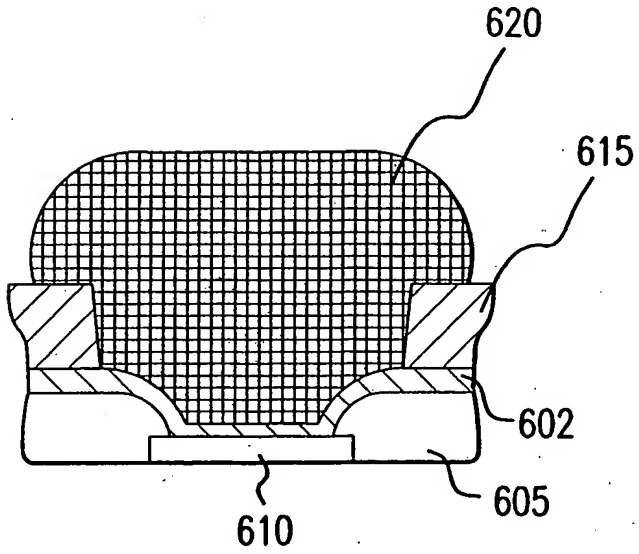

FIG.7

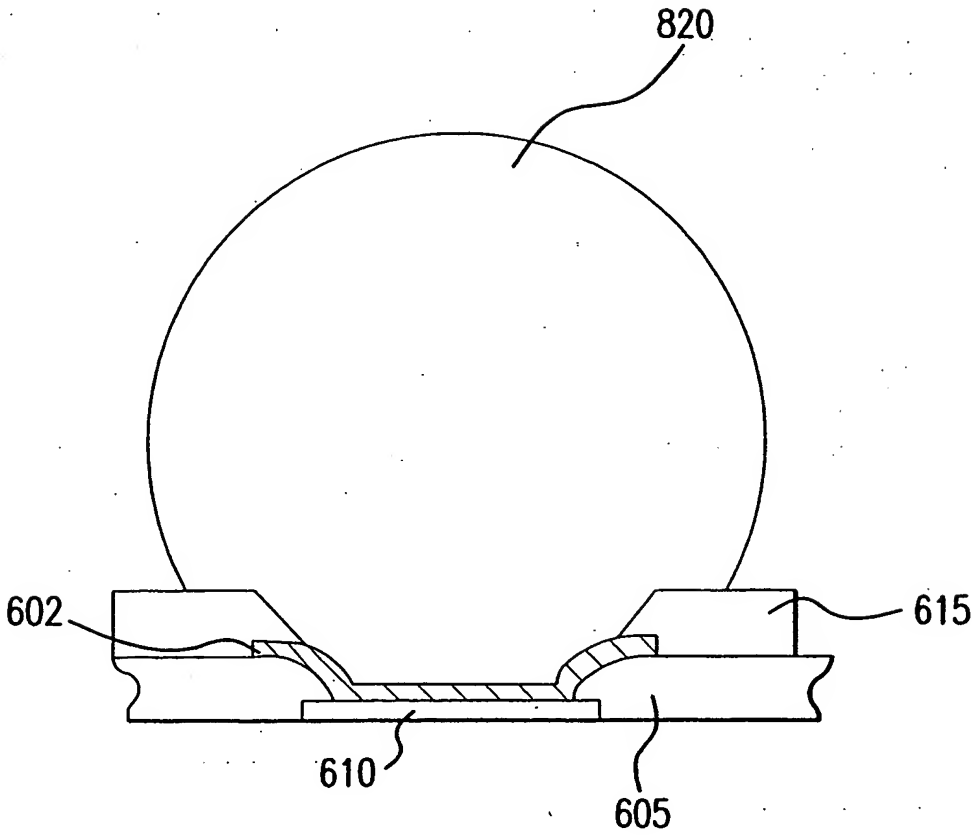

FIG.8

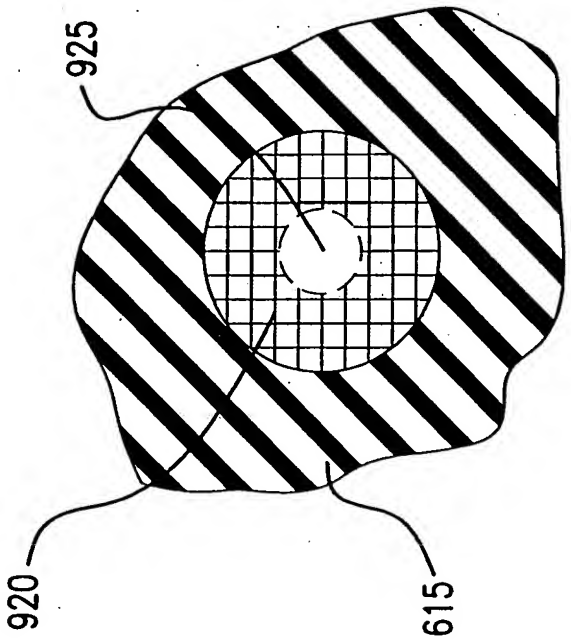

FIG.9B

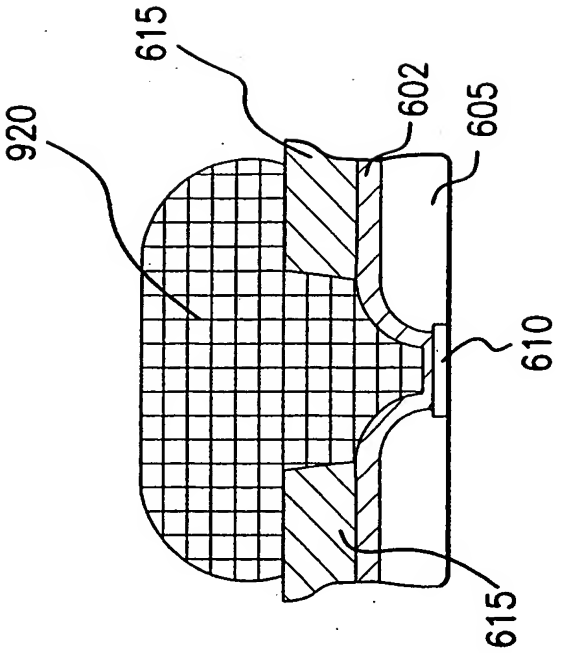

FIG.9A

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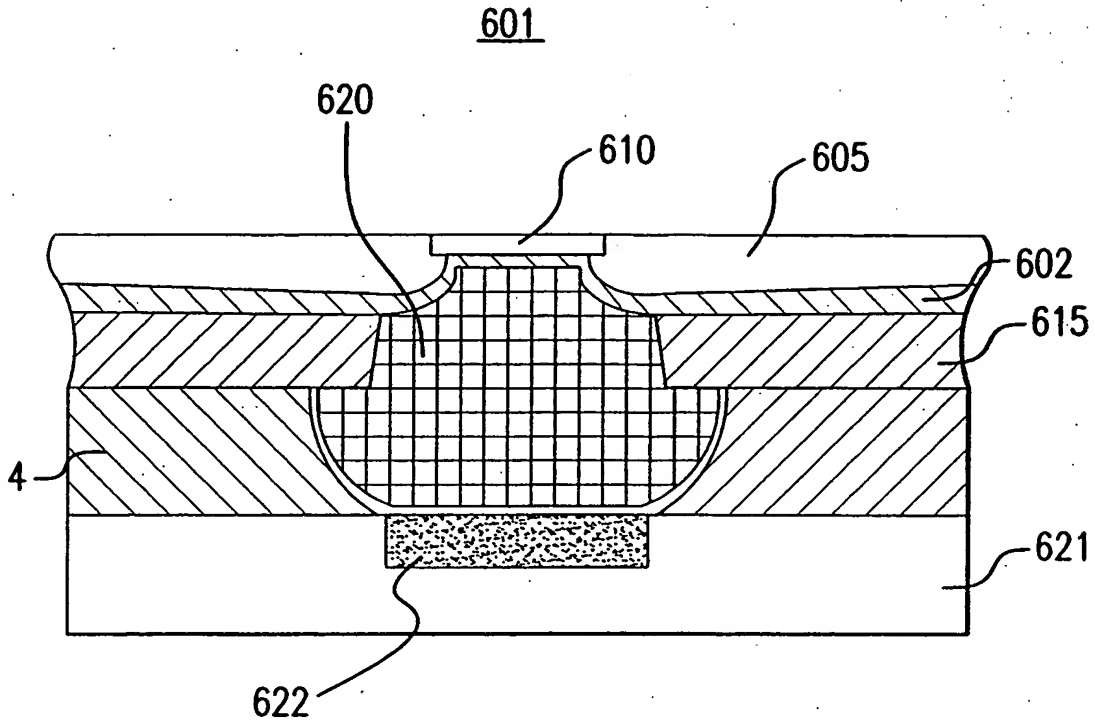

FIG.10

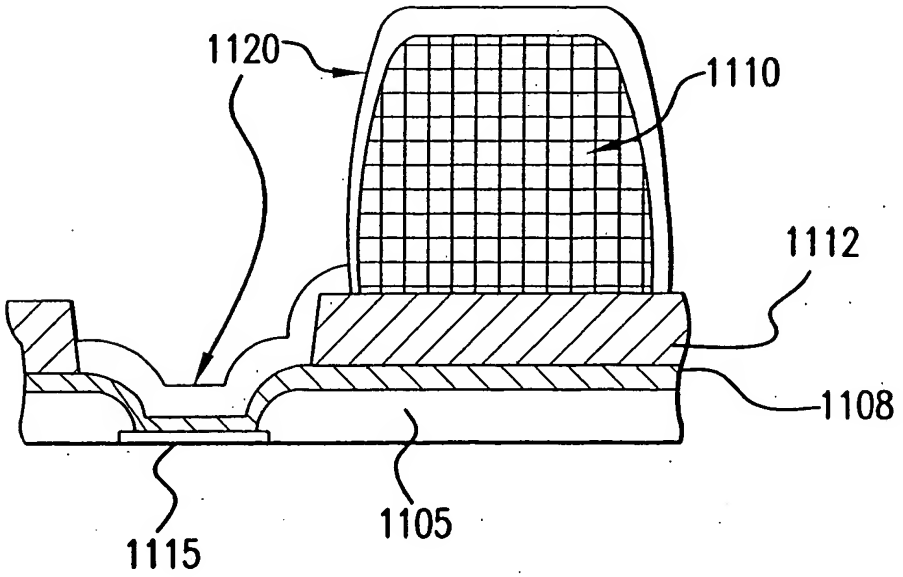

FIG.11

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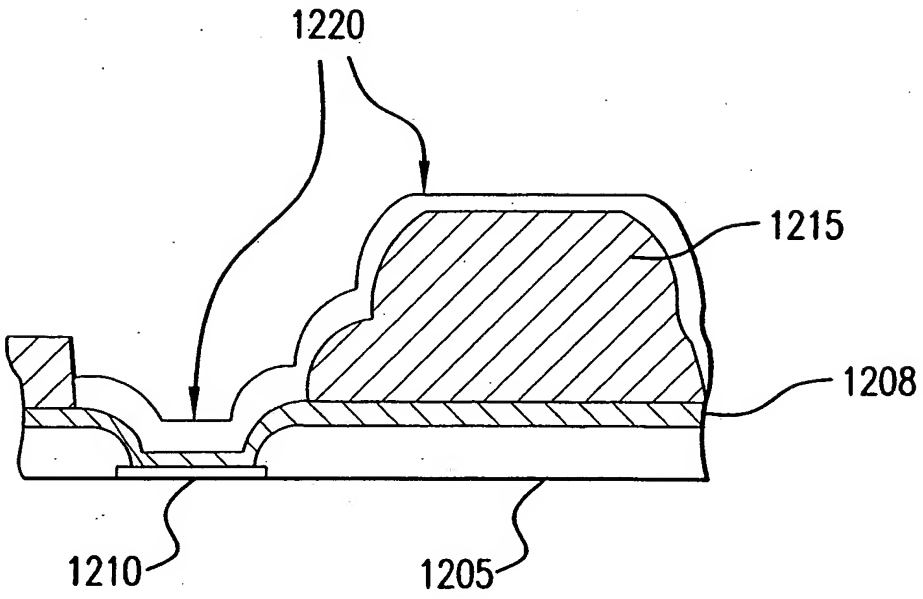

FIG. 12A

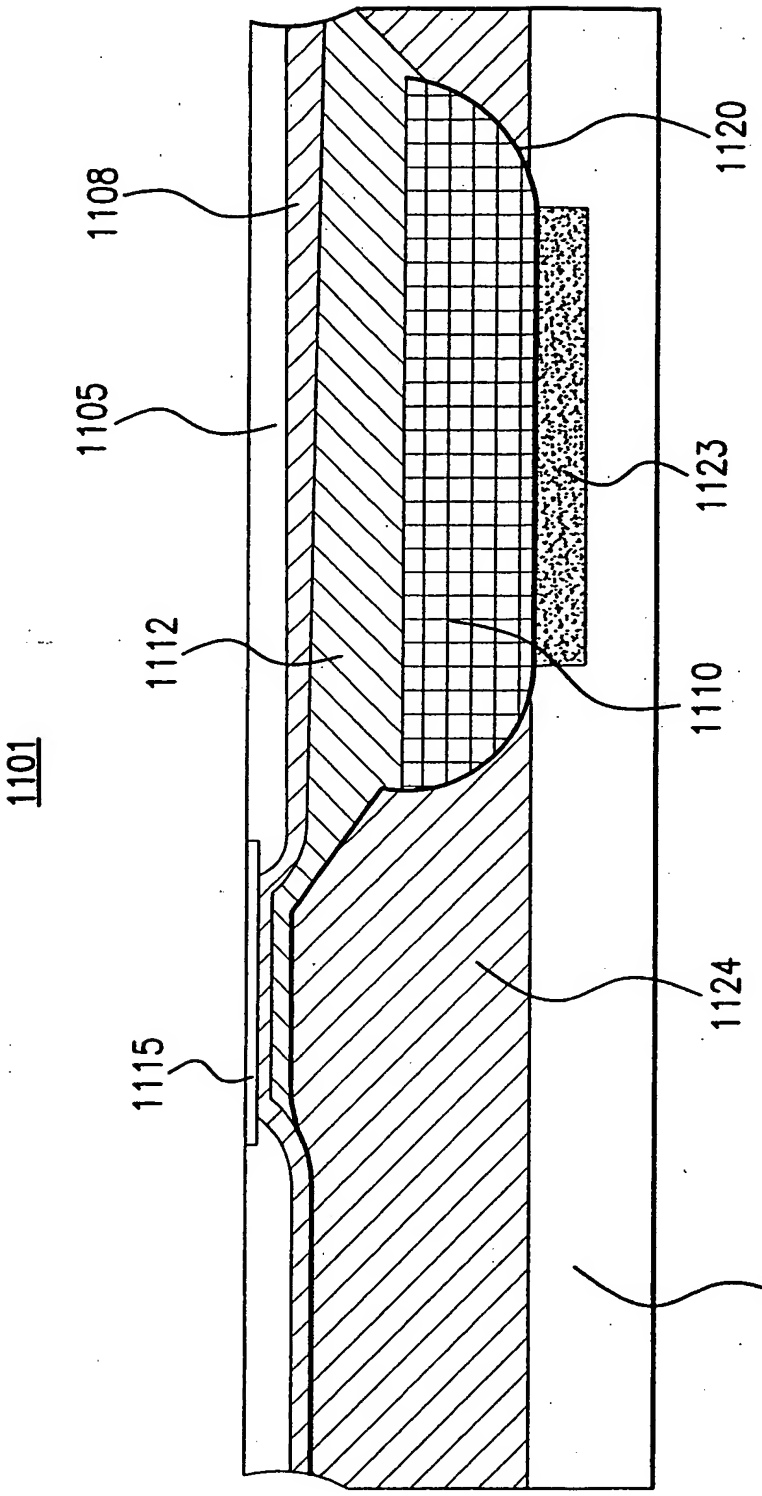

FIG. 12B

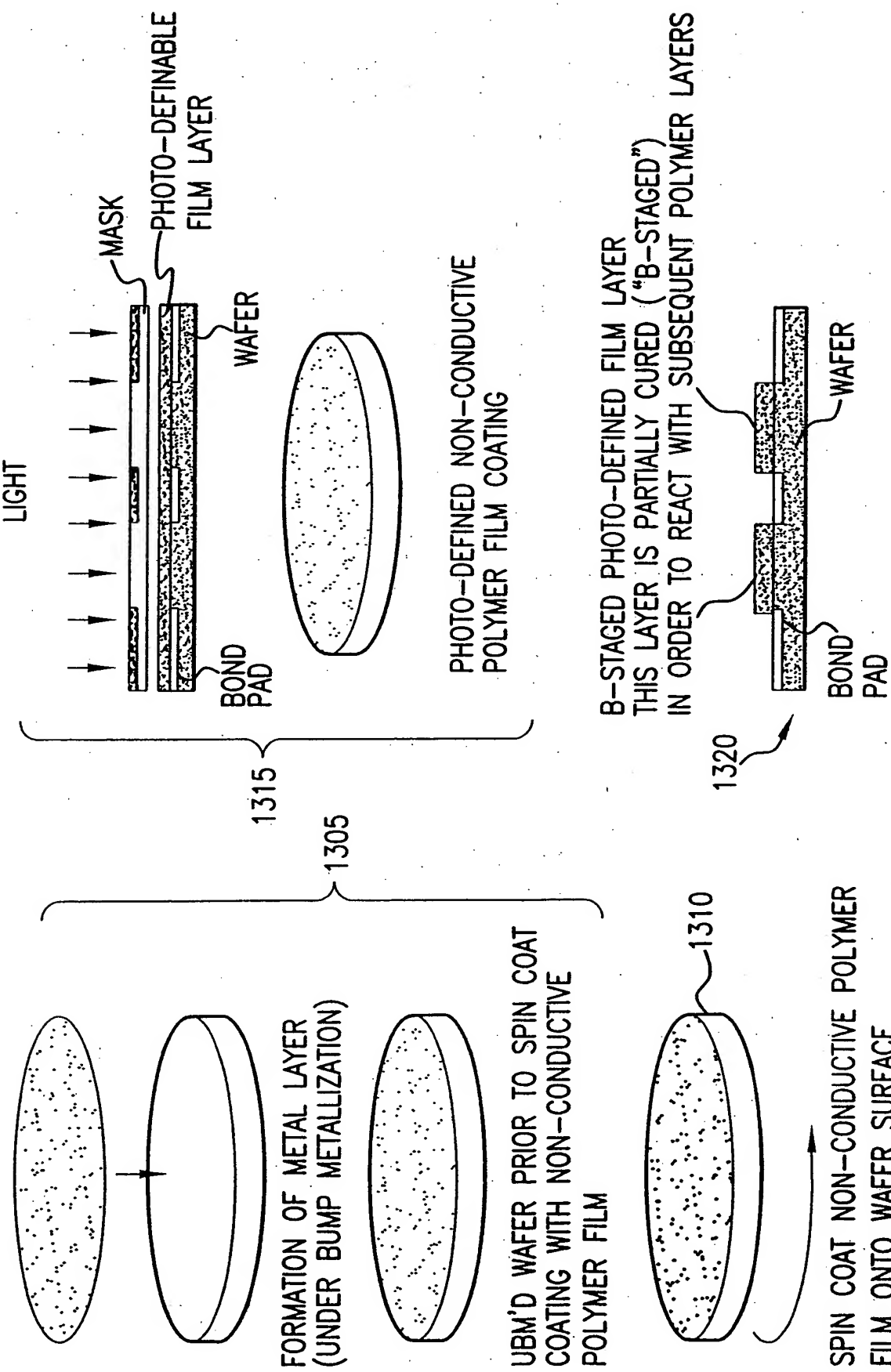
LIGHT
MASK
PHOTO-DEFINABLE FILM LAYER
WAFER
BOND PAD
PHOTO-DEFINED NON-CONDUCTIVE POLYMER FILM COATING
1315
1305
FORMATION OF METAL LAYER (UNDER BUMP METALLIZATION)
UBM'D WAFER PRIOR TO SPIN COAT COATING WITH NON-CONDUCTIVE POLYMER FILM
1310
SPIN COAT NON-CONDUCTIVE POLYMER FILM ONTO WAFER SURFACE
B-STAGED PHOTO-DEFINED FILM LAYER THIS LAYER IS PARTIALLY CURED ("B-STAGED") IN ORDER TO REACT WITH SUBSEQUENT POLYMER LAYERS
WAFER
BOND PAD
1320

FIG.13

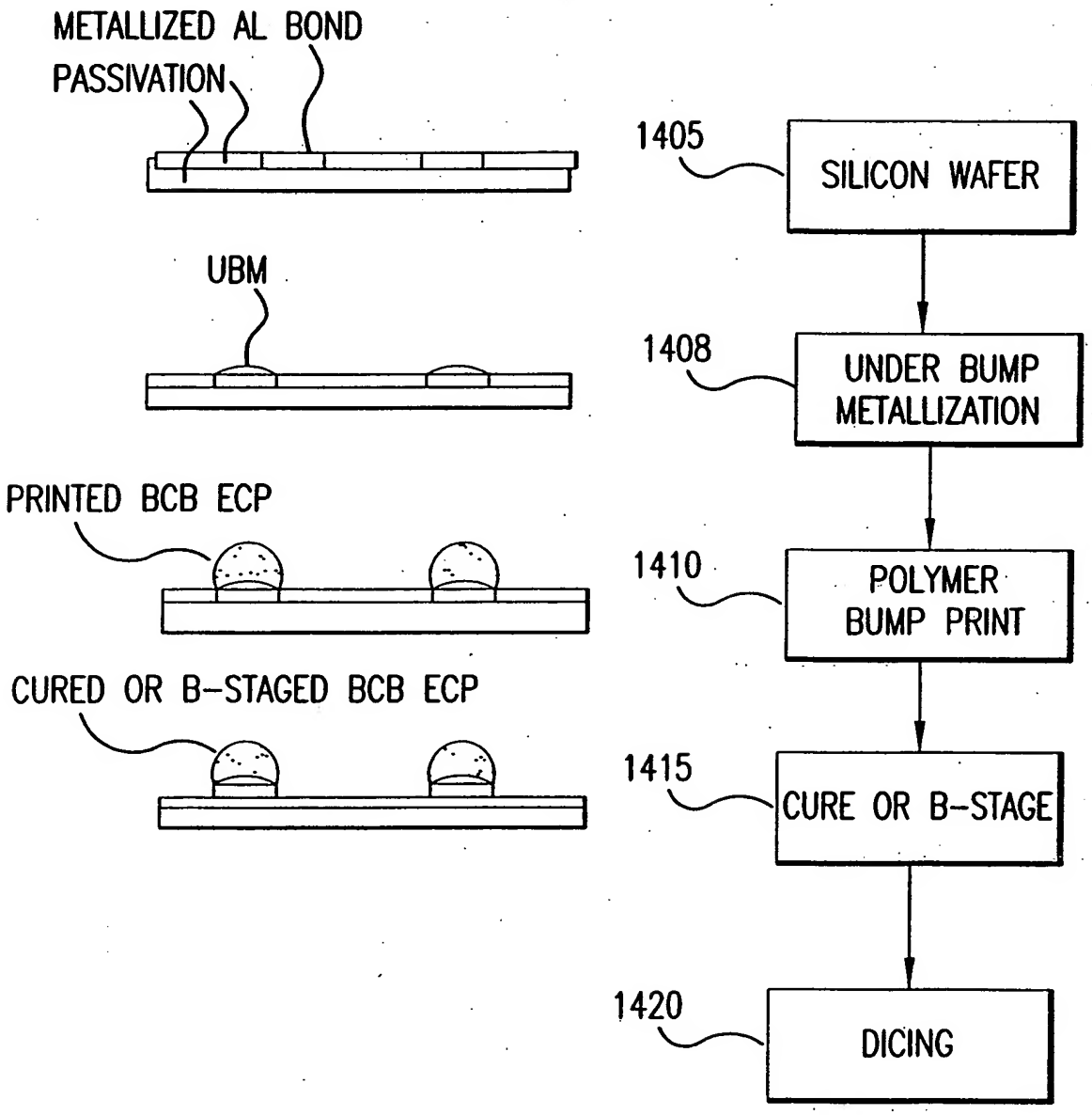
METALLIZED AL BOND
PASSIVATION
UBM
PRINTED BCB ECP
CURED OR B-STAGED BCB ECP
1405
SILICON WAFER
1408
UNDER BUMP METALLIZATION
1410
POLYMER BUMP PRINT
1415
CURE OR B-STAGE
1420
DICING

FIG.14A

1412

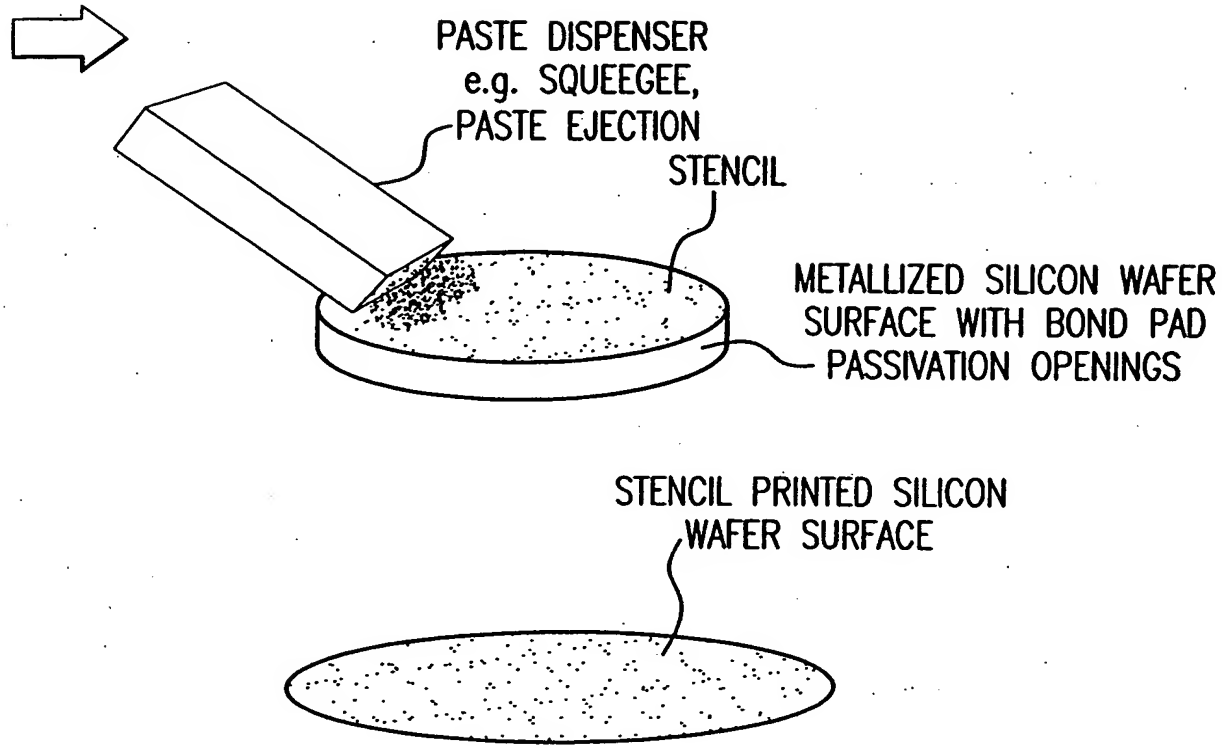

FIG. 14B

1500

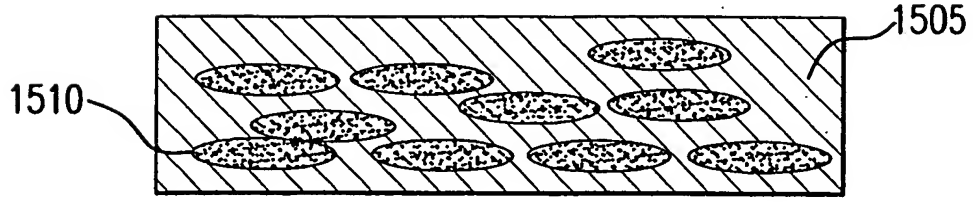

FIG. 15

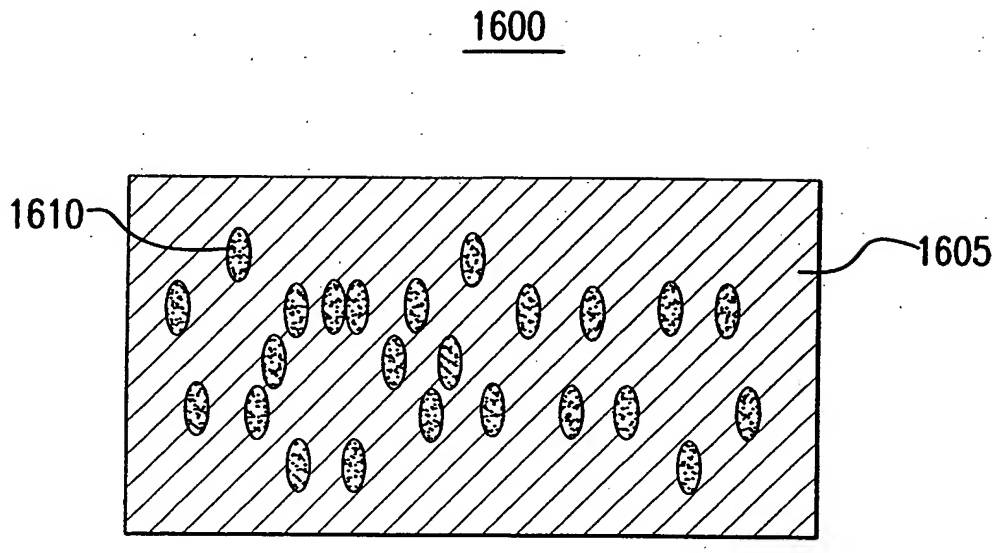

FIG. 16

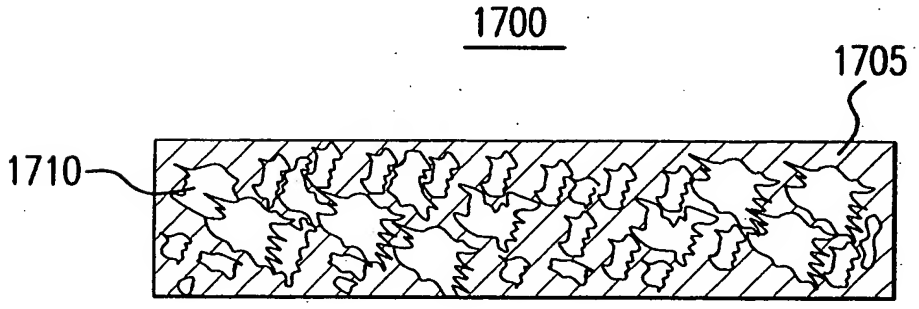

FIG. 17